

a control gate electrode on the interpoly dielectric.

11. (Withdrawn) The method according to claim 10, comprising:

forming silicon oxide sidewall spacers on the side surfaces of the gate structure;

forming a layer of silicon nitride on an upper surface of the gate stack and on the silicon oxide sidewall spacers; and

thereafter depositing the interlayer dielectric.

12. (Currently Amended) A semiconductor device comprising:

a transistor having a gate structure over a substrate with a gate dielectric layer

therebetween;

an interlayer dielectric over the transistor and substrate; and

a silicon-rich silicon oxide layer, having which is substantially opaque to UV radiation and has a refractive index (R.I.) greater than 1.6, on an upper surface of the interlayer dielectric wherein the silicon-rich silicon oxide layer has a thickness of 400Å to 600Å.

13. (Original) The semiconductor device according to claim 12, wherein the silicon-rich silicon oxide layer has a R.I. greater than 1.7.

14. (Original) The semiconductor device according to claim 13, wherein the silicon-rich silicon oxide layer has a R.I. of 1.7 to 2.0.

15. (Cancelled)

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16. (Original) The semiconductor device according to claim 12, wherein the gate structure comprises:

a tunnel oxide as the gate dielectric layer on the substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate electrode on the interpoly dielectric.

17. (Original) The semiconductor device according to claim 16, comprising silicon oxide sidewall spacers on side surfaces of the gate structure.

18. (Original) The semiconductor device according to claim 17, comprising a layer of silicon nitride on an upper surface of the gate structure and on the silicon oxide sidewall spacers.

19. (Original) The semiconductor device according to claim 12, wherein the interlayer dielectric comprises a boron-phosphorous-doped silicate glass (BPSG).

20. (Cancelled)